

#### **TBM Selection Criteria**

Cristian Gingu
- for Fermilab FPIX group -



#### **Parameters' Cut Values**

1. For each test, set the cuts you want to apply. Set also the gain classes (like G300,G500...).

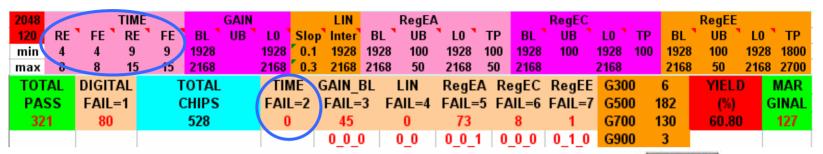
			TIME			GAIN			LIN		RegEA			- 1	RegEC				RegEE		
120	RE	FE	RE 🔭	FE `	BL	UB 🔪	LO `	Slop	Inter	BL	UB `	LO	TP	BL 🔭	UB	` LO `	TP	BL	UB `	LO `	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

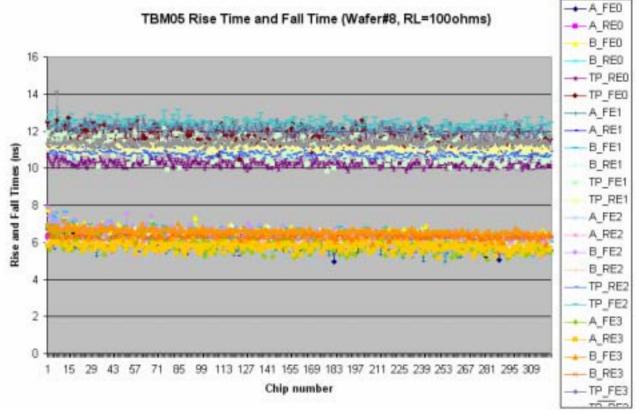
2. Start the code. Load test data files (two files per wafer, analog and digital). The chips passing the above selection are reported.

TOTAL	DIGITAL	TOTAL	TIME	GAIN_BL	LIN	RegEA	RegEC	RegEE	G300	6	YIELD	MAR
PASS	FAIL=1	CHIPS	FAIL=2	FAIL=3	FAIL=4	FAIL=5	FAIL=6	FAIL=7	G500	182	(%)	GINAL
321	80	528	0	45	0	73	8	1	G700	130	60.80	127
				0_0_0	0_0	0_0_1	0 0 0	0_1_0	G900	3		



### **UB and TP Rise and Fall Times**



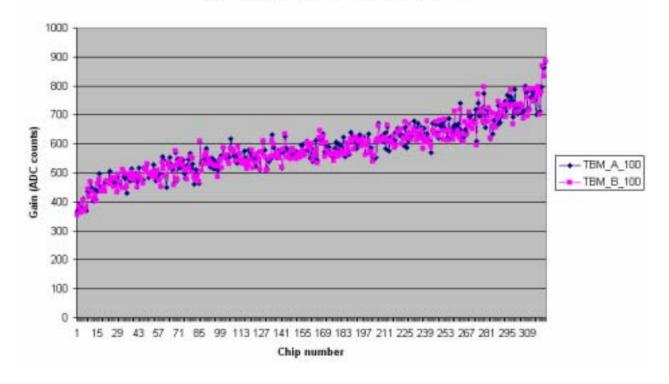




### **Gain Cuts**

2048		٦	TIME			GAIN			LIN		RegEA				RegEC				RegEE		
120	RE	`FE`	RE 🔪	FE/	BL	'UB	LO Ì	Slop	Inter	BL	UB	LO 🔪	TP	BL `	UB	LO 🔪	TP	BL	UB `	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2468		2156	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700
TOT	AL	DIGITA	٨L	T	TOTAL		TIN	IE/(	SAIN_I	BL	LIN	RegE/	A Re	egEC	RegEE	G30	0	6	YIELI	D	MAR
PAS	SS	FAIL=	1	(	CHIPS		FAIL	.=2	FAIL=	3 F	AIL=4	FAIL=	5 FA	AIL=6	FAIL=7	G50	0 1	82	(%)		GINAL
32	1	80			528		0		45		0	73		8	1	G70	0 1	30	60.80	)	127
									000		0_0	0 0 1	0	0 0	0 1 0	G90	0	3			

TBM05 Gain (BL-UB, Wafer#8, RL=100ohms)



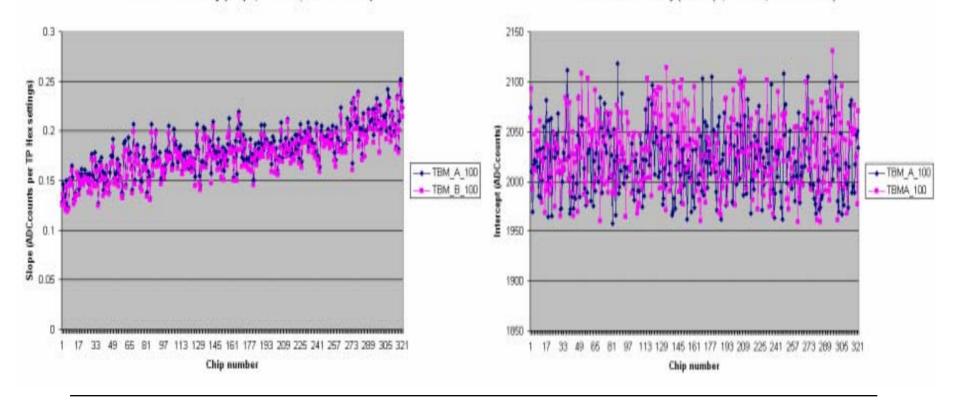


## **TP Linearity Cuts**

2048			TIME			GAIN		LIN		RegE	Δ.			RegEC				RegEE		
120	RE	` FE `	RE 🔪	FE	BL	UB	LO Sic	p Inter	BL	UB	1 L0 1	TP	BL	UB	LO 🔪	TP	BL	UB `	L0	* TP
min	4	4	9	9	1928		1920 0.	1 1928	1928	100	1928	100	1928	100	1928	100	1928	100	192	8 1800
max	8	8	15	15	2168		2168 0.	3 2168	2168	50	2168	50	2168		2168		2168	50	216	8 2700
TO	TAL	DIGIT	AL	Т	OTAL		TIME	GAIN	BŁ	LIN	RegE	A Re	egEC	RegEE	G30	0	6	YIELI	D	MAR
PA	SS	FAIL:	=1	(	CHIPS		FAIL=2	FAIL=	3 F	AIL=4	FAIL=	5 FA	AIL=6	FAIL=7	G50	0 1	82	(%)		GINAL
37	21	80			528		0	45		0	73		8	1	G70	0 1	30	60.80	0	127
								0_0_	0	0 0	0_0_1	0	0_0	0_1_0	G90	0	3			

TBM05 TP Linearity (Slope, Wafer#8, RL=100ohms)

TBM05 TP Linearity (Intercept, Wafer#8, RL=100ohms)



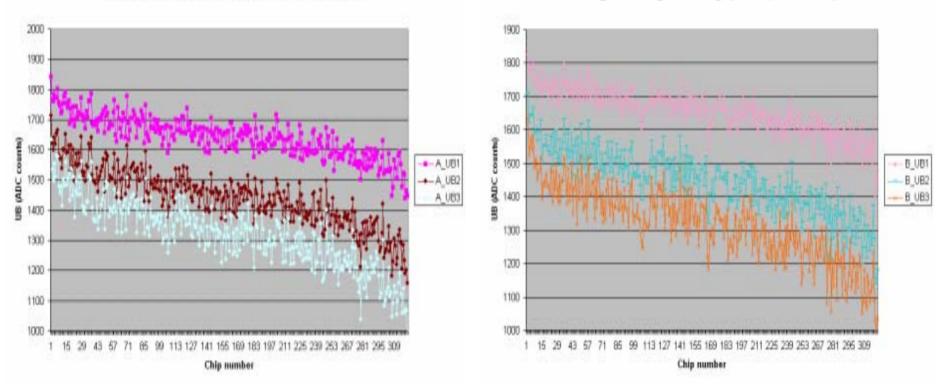


## **TP Register 0xEA Cuts**

2048			TIME			GAIN			LIN		RegEA				RegEC				RegEE		
120	RE	` FE `	RE 1	FE `	BL	UB	LO 🔪	Slop	¹ Inte <mark>/</mark>	BL	UB	LO	TP	BL	UB	LO 🔪	TP	BL	UB `	L0	¹ TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	192	8 1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	216	8 2700
TO	TAL	DIGIT	AL	T	OTAL		TIM	E G	SAIN_	BL	LIN	RegE	A R	egEC	RegEE	G30	0	6	YIELI	D	MAR
P/	SS	FAIL	=1		CHIPS		FAIL	=2	FAIL=	3 F	AIL 4	FAIL=	5 F/	IL=6	FAIL=7	G50	0 1	82	(%)		GINAL
3:	21	80			528		0		45		0	73		8	1	G70	0 1	30	60.80	0	127
									0_0_0	0	0_0	0 0 1	L 0	0_0	0_1_0	G90	0	3			

TBM\_A UB vs Reg0xEA Settings (Wafer#8, RL=100ohms)

TBM\_B UB vs Reg0xEA Settings (Wafer#8, RL=100ohms)

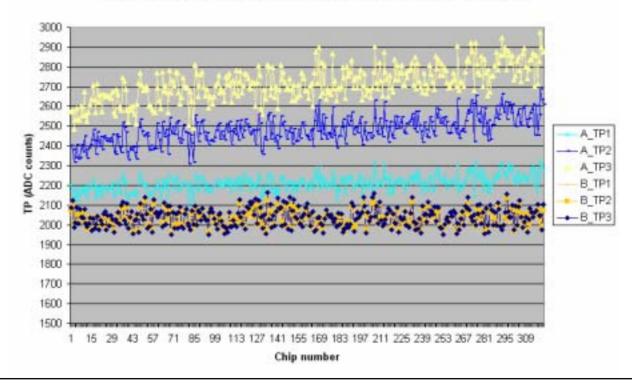




## **TP Register 0xEA Cuts**

2048			TIME			GAIN			LIN		RegE#				RegEC				RegEE		
120	RE	`FE`	RE 🐧	FE `	BL	UB	LO 🔪	Slop	' Inte <mark>/</mark>	BL	UB	LO	TP	BL `	UB	LO 🔪	TP	BL	UB `	L0	* TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1920	8 1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	8 2700
TOT	AL	DIGITA	AL	T	OTAL		TIM	IE G	AIN_	BL	LIN	RegE	A R	egEC	RegEE	G30	0	6	YIELI	D	MAR
PA	SS	FAIL=	:1		CHIPS		FAIL	=2	FAIL=	3 F/	AIL <mark>-</mark> 4	FAIL=	5 FA	IL=6	FAIL=7	G50	0 1	82	(%)		GINAL
32	1	80			528		0		45		0	73		8	1	G70	0 1	30	60.80	0	127
									0_0_0	0	0_0	0 0 1	0	0_0	0_1_0	G90	0	3			

TBM05 TP (applied on P0) vs Reg0xEA Settings (Wafer#8, RL=100ohms)



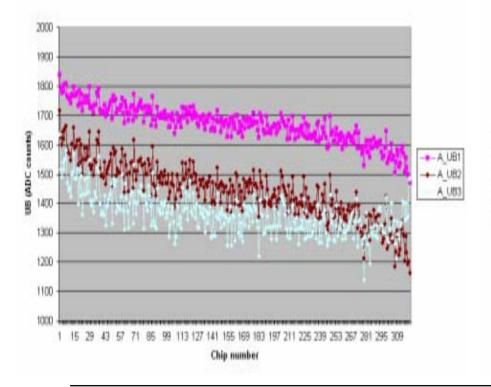


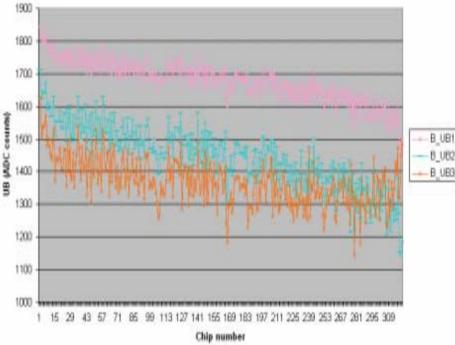
## **TP Register 0xEC Cuts**

2048			TIME			GAIN			LIN		RegEA				RegEC				RegEE		
120	RE	`FE`	RE 🔪	FE	BL 🔪	UB	LO 🔪	Slop	Inter	BL	UB	LO	TP /	BL 🔪	UB 🐧	LO 🔪	TP	BL 🕽	UB `	LO	¹ TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	192	8 1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	216	8 2700
ТОТ	AL	DIGITA	AL	T	OTAL		TIM	IE G	SAIN_I	BL	LIN	RegE	A Re	egEC	RegEE	G30	0	6	YIELI	D	MAR
PA:	SS	FAIL=	-1	(	HIPS		FAIL	=2	FAIL=	3 F/	AIL=4	FAIL=	5 F/	AIL=6	FAIL=7	G50	0 1	82	(%)		GINAL
32	1	80			528		0		45		0	73		8	/1	G70	0 1	30	60.80	0	127
									0_0_0	)	0_0	0_0_	0	0_0	0_1_0	G90	0	3			

TBM\_A UB vs Reg0xEC Settings (Wafer#8, RL=100ohms)

TBM\_B UB vs Reg0xEC Settings (Wafer#8, RL=100ohms)



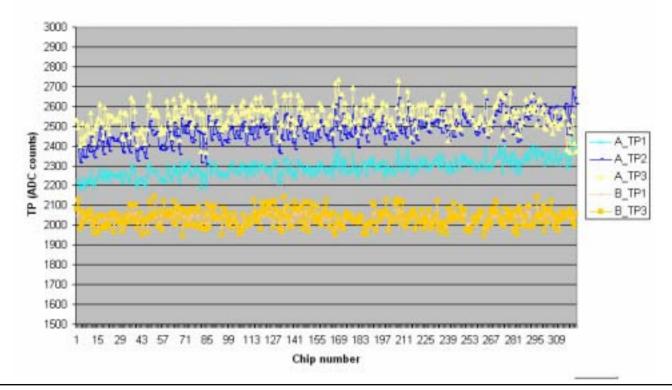




## **TP Register 0xEC Cuts**

204	8			TIME			GAIN			LIN		RegEA				RegEC				RegEE		
120		RE	' FE '	RE 🔪	FE `	BL	UB	LO	Slop	Inter	BL	UB `	LO	TP/	BL 🔪	UB	LO 🔪	TP	BL "	UB 1	L0	TP
mir	1	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	3 1800
ma	х	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	3 2700
TO	)T/	٨L	DIGIT	AL	T	OTAL		TIN	IE G	SAIN_I	BL	LIN	RegE	A R	egEC	RegEE	G30	0	6	YIELD	)	MAR
P.	AS	S	FAIL=	=1	(	CHIPS		FAIL	=2	FAIL=	3 F/	AIL=4	FAIL=	5 F/	AIL=6	FAIL=7	G50	0 1	82	(%)		GINAL
3	321		80			528		0		45		0	73		8	1	G70	0 1	30	60.80	)	127
										0_0_0	)	0_0	0_0_1	0	0_0	0_1_0	G90	0	3			

TBM05 TP (applied on P0) vs Reg0xEC Settings (Wafer#8, RL=100ohms)



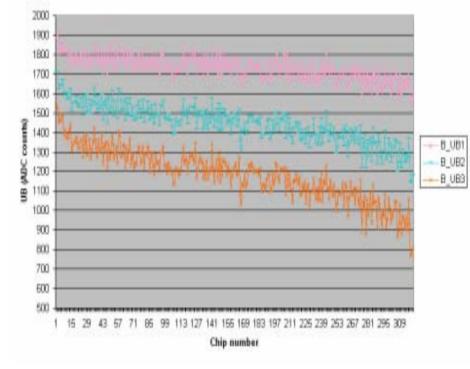


## **TP Register 0xEE Cuts**

2048			TIME			GAIN			LIN		RegE/	1			RegEC				RegEE		
120	RE	`FE`	RE 🔪	FE `	BL 🔪	UB	LO 🔪	Slop	Inter	BL	UB	` L0 `	TP	BL	UB	`LO`	TP/	BL	UB `	LO	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2188	50	2168	2700
TO	ΓAL	DIGIT	AL	T	OTAL		TIM	IE (	SAIN_I	BL	LIN	RegE	A Re	egE <i>C</i>	RegE	E G30	0	6	YIELI	D	MAR
PA	SS	FAIL=	=1	(	CHIPS		FAIL	=2	FAIL=	3 F	AIL=4	FAIL=	5 FA	\II <mark>.</mark> =6	FAIL=	7 G50	0 1	182	(%)	(	GINAL
32	21	80			528		0		45		0	73		8	1	G/0	0 1	130	60.80	)	127
									0_0_0	)	0_0	0_0_1	0	0_0	0_1_0	<b>690</b>	0	3			

TBM\_A UB vs Reg0xEE Settings (Wafer#8, RL=100ohms)

TBM\_B UB vs Reg0xEE Settings (Wafer#8, RL=100ohms)

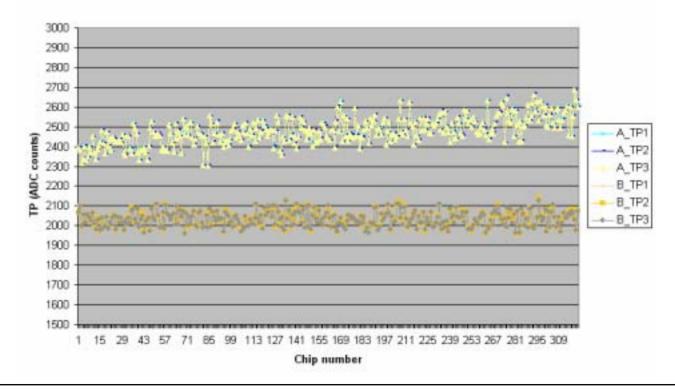




## **TP Register 0xEE Cuts**

2048			TIME			GAIN			LIN		RegE/	4			RegEC	,			RegEE		
120	RE	`FE`	RE 🔪	FE `	BL	UB	LO	Slop	Inter	BL `	UB	` L0 `	TP	BL	UB	`LO`	TP/	BL "	UB `	L0	¹ TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	3 1800/
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2188	50	2168	2700
TO	ΓAL	DIGIT	AL	T	OTAL		TIN	ME (	GAIN_I	BL	LIN	RegE	A Re	egE <i>C</i>	RegE	E G30	0	6	YIELI	D	MAR
PA	SS	FAIL:	=1		CHIPS		FAIL	.=2	FAIL=	3 F	AIL=4	FAIL=	5 F/	\II <mark>.</mark> =6	FAIL=	7 G50	0 1	82	(%)		GINAL
37	21	80			528		0		45		0	73		8	1	G/0	0 1	30	60.80	)	127
									0_0_0	)	0_0	0_0_1	1 0	0_0	0_1_0	<b>690</b>	0	3			

TBM05 TP (applied on P0) vs Reg0xEE Settings (Wafer#8, RL=100ohms)





## **Other Analog Cuts**

 $01\ 000500\ 001500$  'ldig = 5 to 15 mA

 $02\ 000500\ 002500$  'lana = 10 to 25 mA for TBM05,

5 to 15 mA for TBM04

03 001800 002400 'Vcapva = 1.8 to 2.4 V

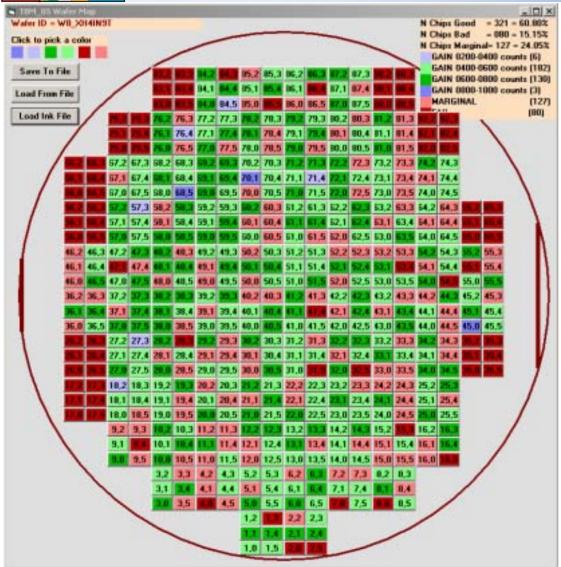
04 001800 002400 'Vcapvd = 1.8 to 2.4 V

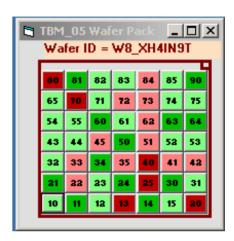
 $05\ 000700\ 001300$  'Vcaplvdslow = 0.7 to 1.3 V

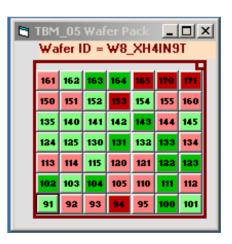
06 000900 001500 'Vcaplvdshigh = 0.9 to 1.5 V



## Wafer Map (Dicing Company)









# **Base Line Cuts Comparison**

204	18			TIME			GAIN			LIN		RegEA				RegEC				RegEE		
12	0 <b>)</b> R	RE 🔪	FE 🔪	RE 🔪	FE `	BL	UB <sup>*</sup>	LO T	Slop	Inter	BL	UB	LO	TP	BL	UB 🔪	LO T	TP	BL	UB	L0	TP
mi	D.	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
ma	X S	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	3 2700
T	IATO	D	IGIT/	AL	T	OTAL		TIN	IE G	SAIN_I	BL	LIN	RegE/	A Re	egEC	RegEE	G30	0	6	YIELI	D	MAR
P	ASS	F	AIL=	:1	(	CHIPS		FAIL	=2	FAIL=	3 F	AIL=4	FAIL=	5 FA	AIL=6	FAIL=7	G50	0 1	82	(%)		GINAL
	321		80			528		0		45		0	73		8	1	G70	0 1	30	60.80	7	127
										0_0_0	)	0_0	0_0_1	0	0_0	0_1_0	G90	0	3			

204	8		T	IME			GAIN			LIN		RegE#	4			RegEC				RegEE		
200	R	E 📜 F	Έ 🔪	RE 🔪	FE `	BL	UB	LO	Slop	Inter	BL	UB	1 L0 1	TP	BL	'UB	LO 🔪	TP	BL	UB	L0	TP
mi	n 4	Į.	4	9	9	1848		1848	0.1	1848	1848	100	1848	100	1848	100	1848	100	1848	100	1848	1800
ma	х 8	3	В	15	15	2248		2248	0.3	2248	2248	50	2248	50	2248		2248		2248	50	2248	2700
TO	TAL	DI	SITA	L	Т	OTAL		TIM	IE G	AIN_E	BL I	LIN	RegEA	Re	egEC	RegEE	G300	)	7	YIELD	)	MAR
P	ASS	F/	\IL=1	ı	C	HIPS		FAIL	=2	FAIL=	3 FA	\IL=4	FAIL=5	FA	AIL=6	FAIL=7	G500	) 2	42	(%)	- 1	GINAL
4	140		80			528		0		0		0	7		0	1	G700	) 1	85	83.33		8
										0 0 0	) (	0 (	0 0 0	0	0 0	0 1 0	G900	)	6			



## **Base Line (Offset) Classes**

C	ffset	2048	TIME			GAIN			LIN	RegEA				RegEC				RegEE				
	Class	120	RE 🔪	FE	RE	FE	BL	UB LO	Slo	p <sup>*</sup> Inter	BL 🔪	UB	LO `	TP	BL	` UB	` L0 `	TP	BL	' UB	LO	¹ TP
	40	min	4	4	9	9	1928		<mark>8</mark> 0.1		1928	100	1928	100	1928	100	1928	100	1928	100	192	8 1800
		max	8	8	15	15	2168	216	<mark>8</mark> 0.3	2168	2168	50	2168	50	2168		2168		2168	50	216	8 2700
	<b>-</b>		DIGIT		_			T1845				_					0000	_		NAME OF		
	TOT	AL	DIGITA	AL	- 1	OTA	L	TIME	GA	IN_BL	LIN	R	egEA	Regi	EC F	RegEE	G300	6		YIELD	)	MAR
	PAS	S	FAIL=	-1	(	CHIPS	S	FAIL=	2 F <i>F</i>	IL=3	FAIL=	4 F	AIL=5	FAIL	=6 F	AIL=7	G500	18	2	(%)		GINAL
	321		80		528			0		45	0		73	8		1	G700	13	0	60.80		127
									0	0_0	0_0	0	0_1	0_0	0	0_1_0	G900	3				

As described in slide 1, chips are assigned different classes based on Gain measurements (like G300 for Gain within 200 and 400 ADC counts). It was suggested to do a similar classification based on offset values.

A chip is assigned an Offset Class depending on Base Line measured values. This is done independently for TBM sections A and B.

If BL class width is defined to be 40 ADC counts (as above), then:

Class 0 <=> BL between (2028,2068)

Class -1 <=> BL between (1988,2028), Class -2 <=> BL between (1948,1988)...

Class 1 <=> BL between (2068, 2108), Class 2 <=> BL between (2108,2148)...

For example, a chip with TBM A Base Line of 2000 ADC counts and TBM B Base Line of 2150 ADC counts will be assigned the class BL-1+3 i.e. the Base Line class is -1 for TBM A and +3 for TBM B.



## **Wafer Report Files**

### After running the code with some selection criteria, the following three files are generated for each wafer:

- 1. A special file used for automatic wafer ink dot placement.
- 2. A special file used for wafer map generation (see slide 13).
- 3. A text file that reports each chip's Gain and Base Line classes. This might be used for TBM chip selection while assembling the modules. It contains (see example below) the testing date, reticule and chip number, a PASS/FAIL string with the test selection criteria that failed, the Gain Class and finally the Base Line Class.

2/28/2006	40	4	<b>PASS</b>	0	<b>G500</b>	BL-2+3
2/28/2006	8	0	<b>PASS</b>	0	<b>G700</b>	<b>BL-1-2</b>
2/28/2006	<b>52</b>	3	PASS	0	G500	BL-2+1
 2/28/2006	54	0	FAIL	1	F1	
2/20/2000	34	U	FAIL	•	FI	
2/28/2006	<b>37</b>	3	FAIL	2	<b>G300</b>	BL-3-1
2/28/2006	14	1	FAIL	3	<b>G500</b>	<b>BL-4-1</b>
2/28/2006	14	5	FAIL	6	G500	BL-3-2
3/1/2006	<b>73</b>	4	FAIL	6	<b>G700</b>	BL-3+2
2/28/2006	<b>39</b>	2	FAIL	<b>32</b>	Ghigh	<b>BL-2-1</b>



### **Base Line Classes Approach**

The TBM Base Line is measured many times while the chip is tested. To assign a Base Line Class, we can use all the available measurements or just some of them. There are seven tests providing base line data: one Gain test (with Test Pulse applied at Port P0), three analog registers (0xEA, 0xEC and 0xEE) scan tests with Test Pulse applied to TBM A Port 0 and another three when the Test Pulse is applied to TBM B Port 2.

We observed that the Base Line value is changing while the analog register settings are changed. This is not a desired effect. To understand how much this affects the Base Line Class assignment we do compare in following four scenarios for class assignment procedure:

- CASE 1. Consider BL data from all seven test and take the worst case value.
- CASE 2. Exclude data from Gain test and consider all register scan tests, regardless of what TBM port the Test Pulse is applied to.
- CASE 3. Consider all six register scan tests but exclude, for each TBM section, the measurements when Test Pulse is applied to that section.
- CASE 4. Same as last scenario and on top of that consider only the BL values measured for default register setting (0x80).

The Base Line histogram obtained from measured data on one wafer are presented in next slides. No significant change can be observed. For conservative reasons, we propose to stick with the most general scenario (CASE 1).



#### **Base Line Classes Scenarios**



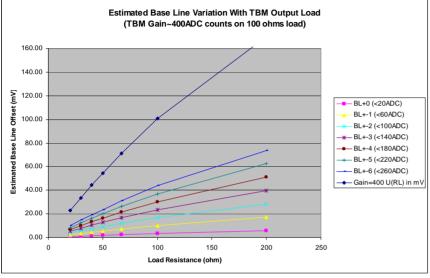


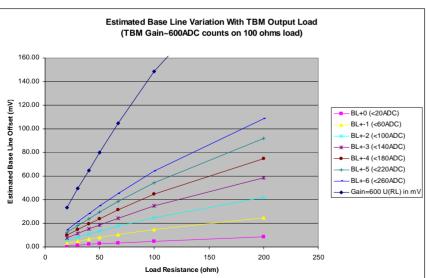
#### **Base Line Classes Scenarios**





# Estimated Base Line Dependence On Load Resistor

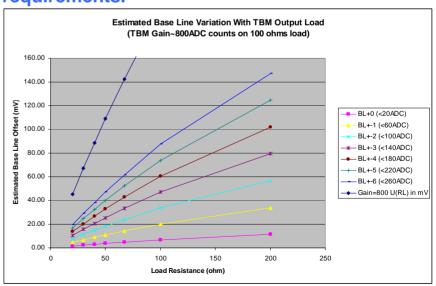




It is difficult to estimate the Base Line Offset for other loads because it is a random value, different for A and B sections and not correlated with Gain measurements.

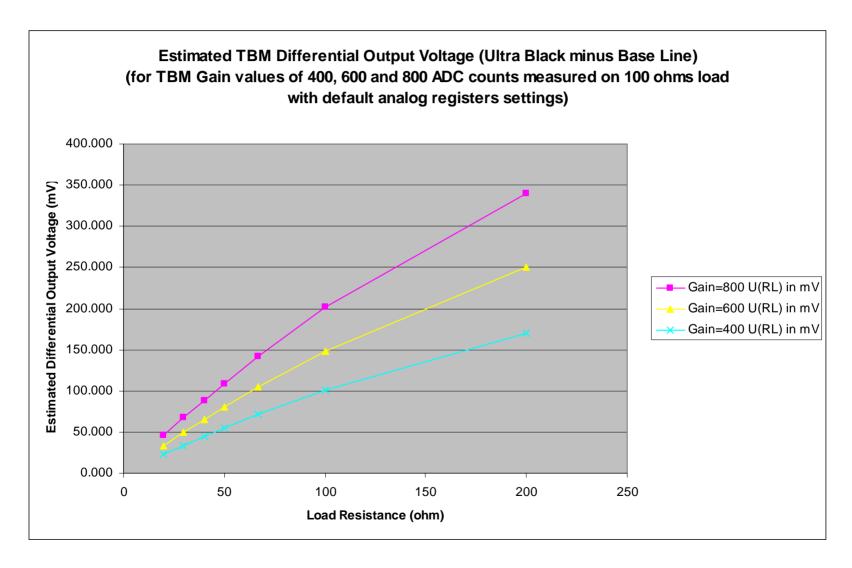
Just for a first order estimate, we'll assume that it will scale down with RL the same way that the TBM Gain does. Using the same calculations presented elsewhere for Gain scaling, the Base Line Offset (mV) will scale as in these graphs.

The right way to impose a cut on accepted BL classes is to provide an absolute voltage offset based on module (system) requirements.





# Estimated Gain Dependence On Load Resistor





# **Base Line Offset Normalized to Gain**

